TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0327US(P8030)

2631 **AF**

In Re Application Of: **Hongjiang Song**

Serial No. 09/473,740	Filing Date 12/28/99	Examiner Don Nguyen Vo	Group Art Unit 2631

Invention: **SYNCHRONIZATION DETECTION ARCHITECTURE FOR SERIAL DATA COMMUNICATION**

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Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **June 11, 2003.**

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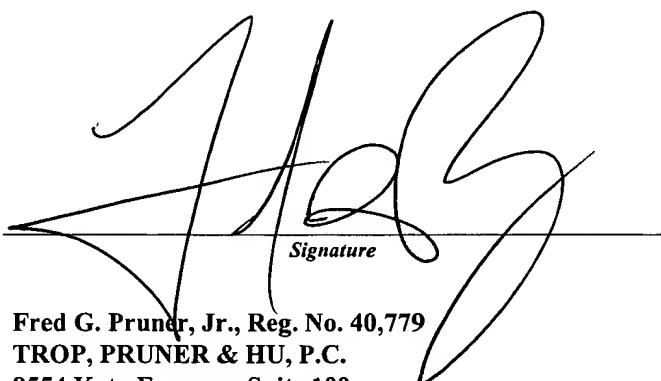
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Hongjiang Song	§	Art Unit:	2631
		§		
Serial No.:	09/473,740	§		
		§	Examiner:	Don Nguyen Vo
Filed:	December 28, 1999	§		
		§		
Title:	Synchronization Detection	§	Docket No.	ITL.0327US
	Architecture for Serial Data	§		(P8030)
	Communication	§		

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APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated March 13, 2003, finally rejecting claims 1-20.

I.   REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010505/0562.

II.   RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III.   STATUS OF THE CLAIMS

Claims 1-20 have been finally rejected and are the subject of this appeal.

IV.   STATUS OF AMENDMENTS

There are no unentered amendments.

V.   SUMMARY OF THE INVENTION

Referring to Fig. 2, an embodiment 30 of a serial bus repeater in accordance with the invention includes a serial bus receiver 33 and a serial bus transmitter 40. The receiver 33 is coupled to a serial bus 32 and may receive, for example, one or more signals that indicate bits of data, and when enabled (as described below), the transmitter 40 generates one or more signals on a serial bus 50 to relay this data. Specification, p. 3.

Serial buses typically are subject to noise and thus, the serial bus communications may be effected by a noisy environment. To minimizing the effects of noise, the repeater 28 includes at least two features to ensure reliable data communication. In particular, the repeater 28 includes a synchronization detection circuit 38 to detect a synchronization field, a bit field used to indicate the beginning of a frame of data, and a squelch circuit 35 to determine whether voltages on the serial bus 32 are indicative of noise or indicate logical levels of data bits. If valid data is being received (as indicated by the squelch circuit 35) and the synchronization detection circuit 38 detects a synchronization field, then the transmitter 40 is enabled to communicate the associated frame of data, a frame that includes the bits of the detected synchronization field and the bits that follow the synchronization field and form the remainder of the frame. Specification, p. 3.

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In a conventional repeater, bits of data that indicate a synchronization field pass through a data recovery circuit and then pass through a synchronization detection circuit, an arrangement that may introduce a significant latency. Unlike the conventional repeater, to detect the synchronization field, the synchronization detection circuit 38 monitors incoming data while the data is propagating through a data recovery circuit 34 (of the repeater 30) thereby reducing the overall latency that may otherwise be introduced by the receiver 30. Thus, due to this arrangement, the overall latency that is introduced by the repeater 30 is the greater of the delay that is introduced by the data recovery circuit 34 or the delay that is introduced by the synchronization detection circuit 38. Specification, p. 3.

In this course of its operation, the data recovery circuit 34 receives one or more signals from the serial bus 32 and converts these signals into indications of bits of data. The data recovery circuit 34 may queue, or buffer, this incoming data for purposes of accommodating different data rates between the incoming data and the outgoing data that is communicated over the serial bus 50. In this manner, if the incoming data is being received at a rate that is higher than the rate at which the transmitter 40 is communicating outgoing data to the serial bus 50, then the data recovery circuit 34 buffers the incoming bits to compensate for the different rates. In some embodiments, while the data recovery circuit 34 is buffering the incoming data, the synchronization detection circuit 38 monitors the buffered data to detect a bit pattern that indicates the synchronization field. Specification, pp. 3-4.

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When the synchronization detection circuit 38 detects the synchronization field, the circuit 38 enables the transmitter 40 to communicate the frame that is associated with the synchronization field over the serial bus 50. In this manner, in some embodiments, after the transmitter 40 communicates a particular frame over the serial bus 50, the transmitter 40 is not again enabled to transmit again until both the synchronization detection circuit 38 indicates the detection of another synchronization field and the squelch circuit 35 indicates that valid logical levels are present on the serial bus 32. When these two conditions occur, the transmitter 40 is enabled to communicate the frame that is associated with the detected synchronization field to the serial bus 50. Specification, p. 4.

In some embodiments, once enabled to transmit, the transmitter 40 receives the bits of the synchronization field (from the data recovery circuit 34) before the other bits of the frame. Thus, the transmitter 40 does not regenerate the synchronization field, but instead, the transmitter 40 relays the buffered synchronization field to the serial bus 50. The transmitter 40 then receives the remaining bits of the frame and communicates these bits to the serial bus 50. Specification, p. 4.

Referring to Fig. 3, in some embodiments, the data recovery circuit 34 may include an analog-to-digital (A/D) interface 60 that receives a clock signal (called CLK_1) from a clock line of the serial bus 32 and other signals from data lines of the serial bus 32. In this manner, on each cycle of the CLK_1 signal, the A/D interface 60 samples and converts two analog data signals from the serial bus 32 into two bits that are received by a fine adjustment delay line 63. The delay line 63 delays the bits to adjust the phase

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between the CLK_1 clock signal of the serial bus 32 and the CLK_2 clock signal of the serial bus 50. The phase adjusted bits subsequently pass into a coarse adjustment delay line 65, a delay line that delays the bits by a multiple number of CLK_2 cycles to accommodate an overall difference in the data rates between the incoming and outgoing data serial buses 32 and 50. In this manner, the coarse adjustment delay line 65 queues, or buffers, the incoming bits to approximately match the rate at which the data is available for transmission to the rate at which the transmitter 40 is communicating the data to the serial bus 50. In some embodiments, a digital signal processing (DSP) engine 62 (of the data recovery circuit 34) adjusts (via control lines 64) the delays that are introduced by the fine adjustment delay line 63 and the coarse adjustment delay line 65. Specification, pp. 4-5.

Referring also to Fig. 4, in some embodiments, the coarse adjustment delay line 65 includes registers 70 (registers 70_1, 70_2, ... 70_{N-1} and 70_N, as examples), each of which may be used to introduce a delay of one CLK_2 clock cycle. As an example, each register 70 may be a D-type flip-flop. In some embodiments, the registers 70 are serially coupled together to form a first-in-first-out (FIFO) that has a fixed output pointer and an adjustable input pointer to allow adjust of the coarse delay. More particularly, in some embodiments, the registers 70 are serially coupled together in the following order: register 70_1 to 70_2 ... to 70_{N-1} to 70_N, with the output terminals 45 of the register 70_N forming output terminals 42 of the coarse delay line 34. The input terminals of each register 70 are coupled to the output terminals of an associated multiplexer 69. In this manner, one set of input terminals of each multiplexer 69 is coupled to input lines 67 of

the delay line 65, and another set of input terminals of each multiplexer 69 (the

multiplexer 69 that is associated with the register 70_1 being the exception) is coupled to

the output terminals 45 of the preceding register 70. The select terminals of the

multiplexers 69 are coupled to the control lines 64. Due to this arrangement, the DSP

engine 62 may use the control lines 64 to select which register 70 receives the input

signals from the lines 67 and thus, control the input pointer in this manner. Specification,

p. 5.

The DSP engine 62 adjusts the coarse delay by moving the input pointer of the

FIFO. For example, the DSP engine 62 may adjust the input pointer to store the data from

the fine adjustment delay line 63 in the registers 70_{N-1} and thus, introduce a two clock

(the CLK_2 clock) delay in the propagation of the incoming data through the coarse delay

line 65. As another example, the DSP engine 62 may move the input pointer to provide

the data from the fine adjustment delay line 63 to the first register 70_1 of the FIFO to

introduce the maximum delay to the data. Specification, p. 5.

The synchronization detection circuit 38 is coupled to a contiguous block of the

registers 70 to detect the synchronization field. For example, the synchronization

detection circuit 38 may be coupled to output terminals 45 of a contiguous group of

registers 70 that includes the last register 70_N. As an example, the synchronization

detection circuit 38 may include a digital comparator that compares the signals that are

provided by the terminals 71 of a selected group of the registers 70 with a predetermined

bit pattern. Based on the result of the comparison, the comparator either asserts (drives

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high, for example) or deasserts (drives low, for example) the line 24 for purposes of selectively enabling or disabling the transmitter 40. Specification, pp. 5-6.

VI.   ISSUES

A.   Can claims 1-7 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

B.   Can claims 1-7 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?

C.   Can claims 8-14 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 8?

D.   Can claims 8-14 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?

E.   Can claim 15-20 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 15?

F.   Can claims 15-20 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?

VII.   GROUPING OF THE CLAIMS

Claims 1-7 can be grouped together; claims 8-14 can be grouped together; and claims 15-20 can be grouped together. With this grouping, all claims of a particular group stand or fall together. Furthermore, regardless of the grouping set forth by the Examiner's rejections, the claims of each group set forth in this section stand alone with respect to the other groups. In other words, any claim of a particular group set forth in this section does not stand or fall together with any claim of any other group set forth in this section.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-7 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

The method of claim 1 includes receiving an indication of bits of incoming data from a first serial bus and buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data. The method includes during the buffering, detecting whether at least some of the bits indicate a synchronization field.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) in view of alleged Applicant's Admitted Prior Art (herein called "AAPA") in view of U.S. Patent No. 5,068,880 (herein called "Kline"). The AAPA to which the Examiner refers is described in the Background section of the present application. The Background section describes a repeater 5 that relays data between two serial buses. The repeater 5 includes a data recovery circuit (DRC) 16 and a synchronization detection circuit 18. The Background section discusses that the DRC 16 buffers incoming receive data to accommodate a difference between a rate at which data is received from a serial bus and a rate at which a transmitter 14 of the repeater 5 communicates data to another serial bus. The AAPA also describes that the synchronization detection circuit 18 receives recovered bits from the DRC 16 and monitors the recovered bits to detect a synchronization field.

Kline generally describes a network 10 that includes a receiver data decoder 38. This data decoder 38, in turn, includes synchronization detection logic 68. *See generally* Figs. 3 and 4A of Kline and the associated text.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for at least the reason that the Examiner fails to show where either the alleged AAPA or Kline allegedly teaches or suggests during the buffering of bits (that accommodates the difference between a first rate of incoming data and a second rate of outgoing data), detecting whether at least some of the bits indicate a synchronization field. More specifically, the alleged AAPA neither teaches nor suggests that the synchronization detection circuit 18, *during* the buffering of bits to accommodate different incoming and outgoing rates, detects whether at least some of the bits indicate a synchronization field. Instead, the synchronization circuit 18 processes bits that are provided by the DRC 16 for purposes of detecting the synchronization field. Therefore, the alleged AAPA teaches detecting the synchronization field *after* buffering to accommodate different rates of data and thus, fails to teach or suggest the detecting of claim 1.

Furthermore, Kline fails to teach or suggest the missing claim limitations. More specifically, Kline teaches a receiver data decoder 38 that includes a register file 56 and a synchronization detection logic 68 that analyzes data in the register file 56 to find word boundaries. Kline, 7:11-26. However, Kline neither teaches nor suggests that the register file 56 is used for purposes of buffering the data to accommodate a difference between incoming and outgoing rates of data. Thus, the Examiner fails to establish a

prima facie case of obviousness for independent claim 1 for at least the reason that the Examiner fails to show where the prior art teaches or suggests detecting a synchronization field *during* buffering of bits to accommodate different incoming and outgoing rates of data.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation combine the alleged AAPA and Kline. A mere conclusion of obviousness based on a combination of references is not sufficient without specific citations to the prior art establishing the suggestion or motivation for the combination. *See Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. Thus, for at least this additional, independent reason, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 1.

Claims 2-7 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, for at least the reasons set forth above, the rejections of claims 1-7 are improper and should be reversed.

B.   Can claims 1-7 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?

The alleged AAPA teaches away from the invention that is set forth by claim 1. More specifically, the Background section (the alleged AAPA) of the present application discloses a data recovery circuit (DRC) 16 that recovers data that is received from a serial

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bus 10 and buffers data to accommodate different data rates. Background, p. 1, ll. 9-15.

The Background also describes a synchronization circuit 18 that receives the recovered

bits from the DRC 16 and monitors these bits to detect a synchronization field. Id., p. 1,

ll. 22-28 and p. 2, ll. 1-3. Thus, the Background section (the alleged AAPA) teaches

away from detecting whether bits indicate a synchronization field *during* the buffering of

the bits to accommodate incoming and outgoing data rates, as the Background section

performing the synchronization field detection *after* this buffering. A reference cannot be

used in a § 103 rejection when the reference teaches away from the claimed invention.

M.P.E.P. § 2145.X.B.

Therefore, for at least this additional, independent reason, the rejections of claims

1-7 are improper and should be reversed.

**C.   Can claims 8-14 be rendered obvious when the Examiner has failed to
         establish a *prima facie* case of obviousness for claim 8?**

The repeater of claim 8 includes a data recovery circuit to receive an indication of

bits of incoming data from a first serial bus and buffer the bits to accommodate a

difference between a first rate of the incoming data and a second rate of outgoing data.

The repeater includes a synchronization detection circuit that is coupled to the data

recovery circuit to detect, while the data recovery circuit is buffering the bit, whether at

least some of the bit indicate a synchronization field.

The Examiner rejects independent claim 8 under 35 U.S.C. § 103(a) as being

obvious over AAPA in view of Kline. However, the Examiner fails to show where either

AAPA or Kline allegedly teaches a synchronization detection circuit to detect whether bits indicate a synchronization field while a data recovery circuit is buffering the bits. In contrast, AAPA teaches detecting a synchronization field after buffering of bits and thus, does not provide the required teaching or suggestion. Kline also fails to teach or suggest detecting a synchronization field during buffering of bits. In this manner, although Kline discloses synchronization detection logic 68, Kline neither teaches or suggests that the synchronization detection logic 68, while a data recovery circuit is buffering bits to accommodate different rates of data, detects a synchronization field in some of these bits.

Thus, for at least the reason that the combination of Kline and the alleged AAPA fails to teach or suggest the synchronization detection circuit of claim 8, a *prima facie* case of obviousness has not been set forth for this claim.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 8 for at least the additional, independent reason that the Examiner does not show wherein the prior art contains the alleged suggestion or motivation to combine Kline and the alleged AAPA. *See Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

Claims 9-14 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, for at least the reason set forth above, the rejections of claims 8-14 are improper and should be reversed.

D. **Can claims 8-14 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?**

The alleged AAPA teaches away from the claimed invention and thus, cannot be used to establish a § 103 rejection of claim 8. M.P.E.P. § 2145X.D. More specifically, the repeater of claim 8 includes a synchronization section circuit to detect, while a data recovery circuit is buffering bits, whether at least some of the bits indicate a synchronization field. Contrary to the limitations of claim 8, the alleged AAPA teaches detecting the synchronization field *after* buffering of the bits to accommodate incoming and outgoing rates of data. Thus, for at least the reason that the alleged AAPA teaches away from the claimed invention, the § 103 rejection of claim 8 is improper.

Therefore, for at least this additional, independent reason, the rejections of claims 8-14 are improper and should be reversed.

E. **Can claim 15-20 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 15?**

The system of claim 15 includes a first serial bus, a second serial bus and a repeater. The repeater is coupled to the first and second serial buses to receive an indication of bits of incoming data from the first serial bus and concurrently buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data and detect whether at least some of the bits indicate a synchronization field.

The Examiner rejects independent claim 15 under 35 U.S.C. § 103 (a) in view of the alleged AAPA and Kline. However, the Examiner fails to show where either the

alleged AAPA or Kline teaches or suggests a repeater to detect whether at least some bits indicate a synchronization field concurrently with the buffering of these bits to accommodate a difference between rates of incoming and outgoing data. Furthermore, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 15 for the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Kline and the alleged AAPA.

Claims 16-20 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, for at least the reasons set forth above, the rejections of claims 15-20 are improper and should be reversed.

F.   Can claims 15-20 be rendered obvious when the alleged admitted prior art teaches away from the claimed invention?

The alleged AAPA teaches a repeater that buffers the bits first and *subsequently* detects a synchronization field. In contrast, the repeater of claim 15 *concurrently* buffers bits to accommodate incoming and outgoing data rates *and* detects a synchronization field in these bits. Thus, the alleged AAPA teaches away from the claimed invention and has been used to improperly reject independent claim 15.

Thus, for at least this additional, independent reason, the rejections of claims 15-20 are improper and should be reversed.

IX.   CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: June 18, 2003
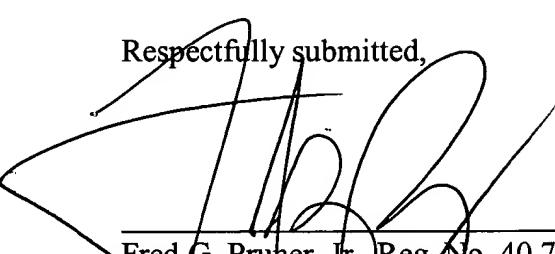
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APPENDIX OF CLAIMS

The claims on appeal are:

1.   A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field.

2.   The method of claim 1, further comprising:

after the buffering, communicating the bits to a second serial bus to form the outgoing data.

3.   The method of claim 2, wherein the communicating comprises:

selectively enabling a transmitter based on the detection.

4.   The method of claim 3, further comprising:

determining whether the indication of the bits indicates valid bit logic levels; and

further basing enablement of the transmitter on the determination.

5.   The method of claim 1, wherein the receiving comprises:

receiving an indication of at least one analog signal from the first serial bus; and

converting the indication of said at least one analog signal into indications of at least

some of the bits.

6.   The method of claim 1, wherein the buffering comprises:

passing the bits through a delay line.

7.   The method of claim 1, wherein the detecting comprises:

comparing at least some of the bits to an indication of a predetermined bit pattern.

8.   A repeater comprising:

a data recovery circuit to receive an indication of bits of incoming data from a first serial

bus and buffer the bits to accommodate a difference between a first rate of the incoming data and

a second rate of outgoing data; and

a synchronization detection circuit coupled to the data recovery circuit to detect, while

the data recovery circuit buffering the bits, whether at least some of the bits indicate a

synchronization field.

9.   The repeater of claim 8, further comprising:

a transmitter to receive an indication of the bits from the data recovery circuit and use the

indication from the data recovery circuit to communicate the bits to a second serial bus to form

the outgoing data.

10.   The repeater of claim 9, wherein the synchronization circuit selectively enables the transmitter based on the detection by the synchronization detection circuit.

11.   The repeater of claim 10, further comprising:

a squelch detection circuit to indicate whether valid bit logic levels are present on the first serial bus,

wherein the synchronization circuit selectively enables the transmitter further based on the indication from the squelch detection circuit transmitter.

12.   The repeater of claim 10, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.

13.   The repeater of claim 10, wherein the data recovery circuit comprises:

a delay line to delay the bits by multiple cycles of a clock signal.

14.   The repeater of claim 10, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

15.   A system comprising:

a first serial bus;

a second serial bus; and

a repeater coupled to the first and second serial busses to receive an indication of bits of

incoming data from the first serial bus, and concurrently buffer the bits to accommodate a

difference between a first rate of the incoming data and a second rate of outgoing data and detect

whether at least some of the bits indicate a synchronization field.

16.   The system of claim 15, wherein the repeater comprises:

a receiver to receive an indication of bits of the incoming data from the first serial bus;

and

a transmitter to communicate the bits to a second serial bus to form the outgoing data.

17.   The system of claim 16, further comprising:

a synchronization circuit to detect the synchronization field and selectively enable the

transmitter in response to the detection.

18.   The synchronization circuit of claim 16, wherein the synchronization detection

circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit

pattern to perform the detection.

19.   The system of claim 15, further comprising:

a squelch detection circuit to enable communication to the second serial bus based on whether valid bit logic levels are present on the first serial bus.

20.   The system of claim 15, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.